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Learn to use Fusion Compiler to perform physical synthesis using the compile_fusion command, which unifies traditional synthesis with placement and optimization, along with additional physical design techniques such as concurrent clock and data optimization.

Fusion Compiler Synthesis - Synopsys

Page 493. Design Compiler Optimization Reference Manual. Design Compiler User Guide. Glossary (= □□□□, □□□□) Slack. A value that represents the difference between the actual arrival time and the required arrival time of data at the path endpoint in a mapped design.. Slack values can be positive, negative, or zero.

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Automated Synthesis from HDL models

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RTL-to-Gates Synthesis using Synopsys Design Compiler

In this tutorial you will use Synopsys Design Compiler to elaborate the RTL for our example greatest common divisor (GCD) circuit, set optimization constraints, synthesize the design to gates, and prepare various area and timing reports. You will also learn how to read the various DC text reports and how to use the graphical

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Synopsys power compiler. Optimize for Power with. 33. Power Compiler Power Compiler always works within the Design Compiler shell and is transparent to Design Compiler users. Synopsys Power Optimizations "tricks" gating clocks of register banks operand isolation. 34. Power Components Leakage Dynamic Switching Internal. 35

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Rtl Compiler User Guide For Flip Flop In this tutorial you will use Synopsys Design Compiler to elaborate the RTL for our example greatest common divisor (GCD) circuit, set optimization constraints, synthesize the design to gates, and prepare various area ... 4 Manual Design Compiler Build Process ... # to verify that latches and flip-flops are ...

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